

WHAT IS CLAIMED IS:

1    1. An integrated circuit comprising:  
2         a substrate having a top surface;  
3         a first dielectric layer formed above the substrate having a trench formed therein,  
4         the first dielectric layer having a first dielectric constant;  
5         a first metal layer formed within the trench of the first dielectric layer;  
6         a second dielectric layer formed above the first metal layer and having a trench  
7         formed therein, the second dielectric layer having a second dielectric constant;  
8         a second metal layer formed within the trench of the second dielectric layer;  
9         a third dielectric layer formed above the second metal layer and having a trench  
10      formed therein, the third dielectric layer having a third dielectric constant; and  
11      a third metal layer formed within the trench of the third dielectric layer.

1    2. The integrated circuit of claim 1 wherein said first dielectric layer has a dielectric  
2         constant of less than 2.8, said second dielectric layer has a dielectric constant of between  
3         2.8 and 3.3, and said third dielectric layer has a dielectric constant of above 3.0.

1    3. The integrated circuit of claim 1 wherein said first dielectric layer comprises a  
2         material selected from the group consisting of an oxide and methylsilsesquioxane  
3         (“MSQ”) hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen  
4         silsesquioxane (“HSQ”) hybrid, an HSQ derivative, and a porogen / HSQ hybrid.

1    4. The integrated circuit of claim 1 wherein said second dielectric layer comprises a  
2         material selected from the group consisting of an oxide and methylsilsesquioxane

3 ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen  
4 silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid .

1 5. The integrated circuit of claim 1 wherein said third dielectric layer comprises a  
2 material selected from the group consisting of silicon glass, undoped silicon glass,  
3 fluorine doped silicon glass, and high-density chemical vapor deposition (HPVCD)  
4 silicon oxide.

1 6. The integrated circuit of claim 1 further comprising a first transistor and a second  
2 transistor formed within the substrate and wherein the first and second transistors are  
3 electrically coupled through the metal layers.

1    7.    A method of forming an integrated circuit comprising:  
2               forming a transistor within a substrate;  
3               depositing a first dielectric material over the transistor;  
4               forming an opening to the transistor in the first dielectric material;  
5               depositing a first metal pattern within the first dielectric material;  
6               depositing a second dielectric material, having a higher dielectric constant than  
7       the first dielectric material, over the first metal pattern;  
8               forming an opening to the first metal pattern in the second dielectric material;  
9               depositing a second metal pattern within the second dielectric material;  
10          depositing a third dielectric material, having a higher dielectric constant than the  
11       first and second dielectric materials, over the second metal pattern;  
12          forming an opening to the second metal pattern in the third dielectric material;  
13          and  
14          depositing a third metal pattern in the third dielectric material.

1    8.    The method of claim 7 wherein depositing a first dielectric material comprises  
2       spin-on depositing a material having a dielectric constant of below 2.8, depositing a  
3       second dielectric material comprises spin-on depositing a material having a dielectric  
4       constant of between 2.5 and 3.3, and depositing a third dielectric material comprises spin-  
5       on depositing a material having a dielectric constant of above 3.0.

1    9.    The method of claim 7 further comprising depositing a fourth dielectric material,  
2       having a higher dielectric constant that is different than the first, second, and third  
3       dielectric materials, over the third metal pattern.

1    10.    The method of claim 7 wherein depositing a first dielectric material comprises  
2    depositing a material selected from the group consisting of an oxide and  
3    methylsilsesquioxane (“MSQ”) hybrid, an MSQ derivative, porogen/MSQa hybrid, an  
4    Oxide / Hydrogen silsesquioxane (“HSQ”) hybrid, an HSQ derivative, and a porogen /  
5    HSQ hybrid.

1    11.    The method of claim 10 wherein depositing a second dielectric material  
2    comprises depositing a material selected from the group consisting of an oxide and  
3    methylsilsesquioxane (“MSQ”) hybrid, an MSQ derivative, porogen/MSQa hybrid, an  
4    Oxide / Hydrogen silsesquioxane (“HSQ”) hybrid, an HSQ derivative, and a porogen /  
5    HSQ hybrid.

1       12. An electrical device comprising:  
2           a plurality of metal layers formed one atop the other;  
3           a plurality of inter-level dielectric layers, each such inter-level dielectric layer  
4       serving to electrically insulate at least one metal layer from at least one other metal layer;  
5       wherein the plurality of inter-level dielectric layers includes:  
6           at a lower region, inter-level dielectric layers having a first dielectric  
7       constant,  
8           at a middle region, inter-level dielectric layers having a second dielectric  
9       constant; and  
10          at an upper region, inter-level dielectric layers having a third dielectric  
11       constant.

1       13. The electrical device of claim 12 wherein:  
2           the first dielectric constant is below 2.8;  
3           the second dielectric constant is between 2.5 and 3.3; and  
4           the third dielectric constant is above 3.0.

1       14. The electrical device of claim 12 wherein the lower region inter-level dielectric  
2       layer comprises a material selected from the group consisting of an oxide and  
3       methylsilsesquioxane (“MSQ”) hybrid, an MSQ derivative, porogen/MSQa hybrid, an  
4       Oxide / Hydrogen silsesquioxane (“HSQ”) hybrid, an HSQ derivative, and a porogen /  
5       HSQ hybrid .

1       15. The electrical device of claim 12 wherein the middle region inter-level dielectric  
2       layer comprises a material selected from the group consisting of an oxide and

3        methylsilsesquioxane (“MSQ”) hybrid, an MSQ derivative, porogen/MSQa hybrid, an  
4        Oxide / Hydrogen silsesquioxane (“HSQ”) hybrid, an HSQ derivative, and a porogen /  
5        HSQ hybrid.

1        16.      The electrical device of claim 12 wherein the upper region inter-level dielectric  
2        layer comprises a material selected from the group consisting of undoped silicon glass,  
3        doped silicon glass, and silicon oxide.

1        17.      The electrical device of claim 12 wherein the first dielectric constant is lower than  
2        the second and third dielectric constants.

1        18.      The electrical device of claim 12 wherein the second dielectric constant is lower  
2        than the first and third dielectric constants.

1        19.      An integrated circuit comprising:  
2                  a substrate;  
3                  a plurality of transistors formed on the substrate;  
4                  a plurality of isolation regions electrically isolating at least one of the plurality of  
5        transistors from at least one other of the transistors;  
6                  a first dielectric layer, having a first dielectric constant, formed above the  
7        substrate having formed therein a via to a transistor, and an interconnect structure;  
8                  a second dielectric layer, having a second dielectric constant, formed above the  
9        first dielectric layer and having formed therein a second interconnect structure; and  
10                 a third dielectric layer, having a third dielectric constant, formed above the second  
11        dielectric layer and having formed therein a third interconnect structure.

1    20.    The integrated circuit of claim 19 wherein the transistors have gate lengths of 130  
2    microns or less.

1    21.    The integrated circuit of claim 19 wherein the substrate is a silicon-on-insulator  
2    substrate.

1    22.    The integrated circuit of claim 19 wherein the first and second dielectric layers  
2    comprise a material selected from the group consisting of an oxide and  
3    methylsilsesquioxane (“MSQ”) hybrid, an MSQ derivative, porogen/MSQa hybrid, an  
4    Oxide / Hydrogen silsesquioxane (“HSQ”) hybrid, an HSQ derivative, a porogen / HSQ  
5    hybrid, nanoporous silica, xerogel, and Poly tetra fluoro ethylene (“PTFE”).

1    23.    The integrated circuit of claim 19 further comprising a first insulator layer  
2    between the substrate and the first dielectric layer.

1    24.    The integrated circuit of claim 19 wherein the via connects to a doped region of a  
2    transistor.

1    25.    The integrated circuit of claim 19 wherein the second dielectric constant is lower  
2    than the third dielectric constant and the first dielectric constant is lower than both the  
3    second and third dielectric constants.